JC4-905

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U.S. **UTILITY** Patent Application

PATENT NUMBER and ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10032646	12/27/2001	257	314	2811	Luke

**APPLICANTS: Randolph Mark;

**CONTINUING DATA VERIFIED:
none
Luke

** FOREIGN APPLICATIONS VERIFIED:
none
Luke

PG-PUB DO NOT PUBLISH ☒ RESCIND ☐

Foreign priority claimed	☐ yes ☑ no	ATTORNEY DOCKET NO
35 USC 119 conditions met	☐ yes ☑ no	G0727/2243P
Verified and Acknowledged Examiners's intials	Luke	

TITLE : Planar transistor structure using isolation implants for improved Vss resistance and for process simplification

U.S DEPT. OF COMM /PAT & TM-PTO-436L(Rev 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
	Assistant Examiner	Total Claims	Print Claim for O.G
ISSUE FEE		DRAWING	
Amount Due / Date Paid		Sheets Drwg. / Figs.Drwg. / Print Fig.	
☐ TERMINAL DISCLAIMER	Primary Examiner	Application Examiner	
	PREPARED FOR ISSUE		

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